METHOD AND APPARATUS FOR TRANSFERRING DATA BETWEEN A SOURCE REGISTER AND A DESTINATION REGISTER

Abstract of the Disclosure

A circuit selectively extracts bits from different locations from a source register and loads them in logical order in one side of a destination register. The register is divided into subsets. All of the transfer bits in each subset are arranged on one side and in logical order. These subsets are paired. The bits from one pair are shifted by an amount equal to the non-transfer bits from the other pair and then combined with the bits from the other pair to form a new group of bits that are on one side and are in logical order. The process of shifting bits of one of a pair of groups and combining with the other of the pair continues until all of the transfer bits from the source register are in one group on one side and in logical order.